CLAIMS

What is claimed is:

1. A method for utilizing a signal delay model for determining an interconnect delay at a node in an interconnect having a plurality of nodes, said method comprising:

determining an equivalent effective capacitance value for a downstream load seen at said node; and

utilizing said equivalent effective capacitance value to calculate said interconnect delay at said node.

2. The method as recited in Claim 1, further comprising performing a bottom-up tree traversal to compute the first three admittance moments for each of said plurality of nodes in said interconnect.

3. The method as recited in Claim 1, wherein said determining an equivalent effective capacitance value includes determining interconnect delays for nodes in said interconnect preceding said node.

4. The method as recited in Claim 1, wherein said determining an equivalent effective capacitance includes utilizing a pi-model to model said downstream load.

5. The method as recited in Claim 4, wherein said determining an equivalent effective capacitance includes determining an Elmore delay value for said node.

6. The method as recited in Claim 5, wherein said

equivalent effective capacitance (C_{eff}) is characterized by:

$$C_{eff} = C_{fj}(1 - e^{-T/\tau dj})$$

wherein C_{fj} is the far-end capacitance of said pi-model at said node, T is the Elmore delay at said node and τdj is the resistance of said pi-model (R_{dj}) multiplied by C_{fj}.

7. The method as recited in Claim 6, wherein said utilizing said equivalent effective capacitance value includes calculating said interconnect delay at said node utilizing an effective capacitance metric (ECM) delay model, wherein said ECM delay model is characterized by:

$$ECM_j = ECM_{p(j)} + R_j(C_j + C_{nj} + C_{fj}(1 - e^{-T/\tau dj}))$$

wherein $ECM_{p(j)}$ is the computed ECM delay at the node immediately preceding said node, R_j is the resistance between said node and said preceding node, C_j is the capacitance to ground at said node and C_{nj} is the near-end capacitance of said pi-model at said node.

8. A data processing system, comprising:

a processor;

means for determining an equivalent effective capacitance value for a downstream load seen at a node in an interconnect having a plurality of nodes; and

means for utilizing said equivalent effective capacitance value to calculate an interconnect delay at said node.

9. The data processing system as recited in Claim 8, further comprising means for performing a bottom-up tree traversal to compute the first three admittance moments for each of said plurality of nodes in said interconnect.

10. The data processing system as recited in Claim 8, wherein said means for determining an equivalent effective capacitance value includes means for determining interconnect delays for nodes in said interconnect preceding said node.

11. The data processing system as recited in Claim 8, wherein said means for determining an equivalent effective capacitance includes means for utilizing a pi-model to model said downstream load.

12. The data processing system as recited in Claim 11, wherein said means for determining an equivalent effective capacitance includes means for determining an Elmore delay value for said node.

13. The data processing system as recited in Claim

12, wherein said equivalent effective capacitance (C_{eff}) is characterized by:

$$C_{eff} = C_{fj}(1 - e^{-T/\tau dj})$$

wherein C_{fj} is the far-end capacitance of said pi-model at said node, T is the Elmore delay at said node and τdj is the resistance of said pi-model (R_{dj}) multiplied by C_{fi}.

14. The data processing system as recited in Claim 13, wherein said means for utilizing said equivalent effective capacitance value includes means for calculating said interconnect delay at said node utilizing an effective capacitance metric (ECM) delay model, wherein said ECM delay model is characterized by:

$$ECM_j = ECM_{p(j)} + R_j(C_j + C_{nj} + C_{fj}(1 - e^{-T/\tau dj}))$$

wherein $ECM_{p(j)}$ is the computed ECM delay at the node immediately preceding said node, R_j is the resistance between said node and said preceding node, C_j is the capacitance to ground at said node and C_{nj} is the near-end capacitance of said pi-model at said node.

15. A computer program product, comprising: a computer-readable medium having stored thereon computer executable instructions for implementing a method for determining an interconnect delay at a node in an interconnect having a plurality of nodes, said computer executable instructions when executed perform the steps of:

determining an equivalent effective capacitance value for a downstream load seen at said node; and

utilizing said equivalent effective capacitance value to calculate said interconnect delay at said node.

16. The computer program product as recited in Claim 15, further comprising performing a bottom-up tree traversal to compute the first three admittance moments for each of said plurality of nodes in said interconnect.

17. The computer program product as recited in Claim 15, wherein said determining an equivalent effective capacitance value includes determining interconnect delays for nodes in said interconnect preceding said node.

18. The computer program product as recited in Claim 15, wherein said determining an equivalent effective capacitance includes utilizing a pi-model to model said downstream load.

19. The computer program product as recited in Claim 18, wherein said determining an equivalent effective capacitance includes determining an Elmore

delay value for said node.

20. The computer program product as recited in Claim 19, wherein said equivalent effective capacitance (C_{eff}) is characterized by:

$$C_{eff} = C_{fj}(1 - e^{-T/\tau dj})$$

wherein C_{fj} is the far-end capacitance of said pi-model at said node, T is the Elmore delay at said node and τdj is the resistance of said pi-model (R_{dj}) multiplied by C_{fi}.

21. The computer program product as recited in Claim 20, wherein said utilizing said equivalent effective capacitance value includes calculating said interconnect delay at said node utilizing an effective capacitance metric (ECM) delay model, wherein said ECM delay model is characterized by:

$$ECM_j = ECM_{p(j)} + R_j(C_j + C_{nj} + C_{fj}(1 - e^{-T/\tau dj}))$$

wherein $ECM_{p(j)}$ is the computed ECM delay at the node immediately preceding said node, R_j is the resistance between said node and said preceding node, C_j is the capacitance to ground at said node and C_{nj} is the near-end capacitance of said pi-model at said node.